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ABSTRACT

We propose a new microwave power divider/combiner with multiple-port double-ladder structure for use in high power solid-state power amplifiers. Numerical and experimental analysis were carried out at X-band, and the results of the divider/combiner indicated low insertion loss and wide band characteristics in good accordance with the theory.

INTRODUCTION

Microwave solid-state high power amplifiers are typically composed of three stages : division of a signal to be amplified, amplification of each divided signal and combining of amplified signals. To obtain higher output power and wide-band characteristics, it is required to develop a multiple-port power divider/combiner with low insertion loss and wide-band characteristics. In this paper, we propose a microwave power divider/combiner with multiple-port double-ladder structure for use in high power solid state power amplifiers.

The ladder structure refers to a rectangular waveguide having an array of paired coaxial probes placed symmetrically with the guide axis. The double-ladder structure consists of a coaxial input/output probe in the middle of the waveguide and two same ladder structures placed at both side of the center coaxial probe (Fig. 1). By using waveguide, the divider/combiner can handle high power and create less loss than those using strip line. Also, the divider/combiner can be designed so as to have wideband characteristics with little standing wave ingredients. Moreover, because the divider/combiner is regarded as a parallel-running two single-ladder structure[1], it is expected to be capable of doubling the number of ports without deteriorating the characteristics.

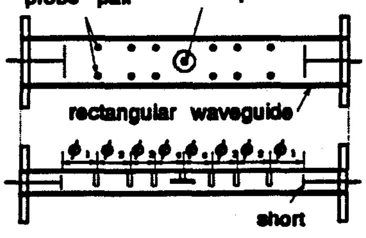

Fig. 1 Divider/combiner with double-ladder structure (upper : top view, lower : side view).

DESIGN FOR PERFECT POWER DIVISION/COMBINING

It is possible for the divider/combiner to divide the input power equally with no reflection loss at the input port, and to combine $4N$ equal-amplitude inputs completely.

Fig. 2 shows the equivalent circuit of the double-ladder divider. It is assumed in the analysis that incoming wave propagates only in the dominant mode. The circuit represents the right side alone of the divider since the divider is symmetrical with the center probe. ϕ_k's ($1 \leq k \leq N$) are electric lengths between neighboring probe-pairs, $y_p = g_p + jb_p$ is the admittance of a probe-pair, and $y_L = g_L + jb_L$ is the admittance looking from N-th probe-pair to the left, each admittance being normalized by the characteristic admittance of the waveguide. Denoting the current source as $i_{in} = I_{in} \exp\{j(\omega_0 t + \psi)\}$, voltages of k-th ($1 \leq k \leq N$) node as $v_k = V_k \exp\{j(\omega_0 t + \varphi_k)\}$, we can obtain the following equation,

$$\begin{aligned} jb_{tk}V_{k-1}e^{-j\varphi_{k,k-1}} + (g_p + \delta_{kN}g_L + jb_k)V_k \\ +jb_{t,k+1}V_{k+1}e^{j\varphi_{k+1,k}} &= \delta_{kN}Y_0^{-1}I_{in}e^{j(\psi-\varphi_N)} \\ &(1 \leq k \leq N) \quad (1) \end{aligned}$$

where,

$$b_k = \begin{cases} -\cot\phi_k + b_p - \cot\phi_{k+1} & (1 \leq k \leq N-1) \\ -\cot\phi_N + b_p + b_L & (k = N) \end{cases} \quad (2)$$

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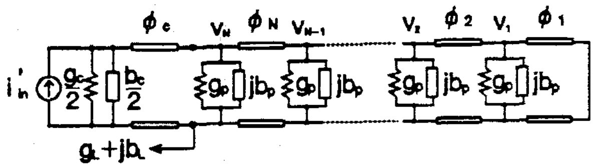

Fig. 2 Equivalent circuit of the divider.

$$b_{tk} = \begin{cases} 0 & (k = 1 \text{ or } N+1) \\ \mathrm{cosec}\phi_k & (2 \le k \le N) \end{cases} \quad (3)$$

$$\varphi_{mn} = \varphi_m - \varphi_n \quad (4)$$

and δ_{kN} is the Kronecker's delta :

$$\delta_{kN} = \begin{cases} 1 & (k = N) \\ 0 & (k \ne N). \end{cases} \quad (5)$$

Taking two conditions into account to divide the signal with no reflection loss at the input port 1) the available power of the input current source is equal to the sum of powers $(1/2)g_p Y_0 V_k{}^2$ provided to each conductance g_p, and 2) all the node voltages are equal; i.e., $V_1 = V_2 = \cdots = V_N$, the design formula for perfect power division is given as

$$g_L = N g_p \quad (6)$$

$$b_L = -b_p/2 \quad (7)$$

$$-\cot\phi_1 = -b_p/2 \quad (8)$$

$$-\cot\phi_k = \frac{1}{b_p}\{1-(\frac{b_p}{2})^2-(k-1)^2 g_p^2\} \ (2 \le k \le N). \quad (9)$$

For the design of the combiner, similar equivalent circuit is available, and it is derived that the perfect power combining can be attained when all amplitudes of the input signals are equal and their phases Ψ_k's $(1 \le k \le N)$ satisfy the following relation:

$$\sin(\Psi_k - \Psi_{k-1}) = -(k-1)g_p \sin\phi_k. \quad (10)$$

The design formula for perfect power combining is expressed by the same expression as equations (6) $\sim$ (9) completely. Therefore, the divider and the combiner have the same structure.

The design formula (6) and (7) provide the load admittance $y_L = g_L + jb_L$ looking from the last probe-pair, but this design is not unique; i.e., y_L depends on the admittance $y_c = g_c + jb_c$ and the distance ϕ_c. Note that the half of the admittance of center probe $y_c/2$ should be matched to y_L with the distance ϕ_c, i.e.:

$$y_c = 2\frac{y_L - j\tan\phi_c}{1 - jy_L\tan\phi_c}. \quad (11)$$

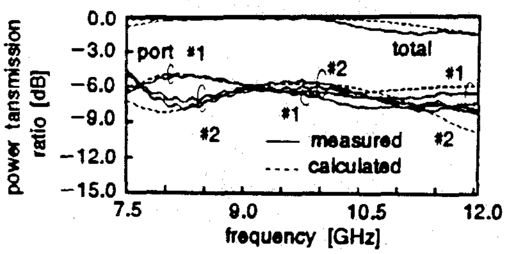

Fig. 3 Frequency characteristics of the 8-way divider.

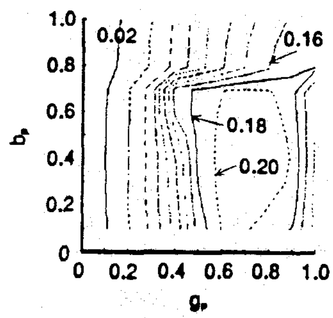

Fig. 4 -0.5dB-relative bandwidth r on the admittance of the probe-pair (8-way divider).

It is convenient that the ϕ_c is selected as short as possible so as to minimize the frequency dependance, though the size of the connector of the input/output port may limit it.

NUMERICAL ANALYSIS AND EXPERIMENTS FOR POWER DIVISION

Numerical analysis for wideband characteristics

Numerical analysis was carried out so as to investigate the frequency characteristics using (1). The center probe is designed as $g_c + jb_c = 2y_L$ with $\phi_c = \pi$ to satisfy (11) at 9.0GHz. Fig.3 shows the frequency characteristics of the ratio of the output power of each probe-pair to the input power for 8-way ($N = 2$) divider and the divider efficiency defined by the total output power relative to the input power. It is noted that equal amplitude and perfect power division are realized at the designed frequency f_0. The efficiency deteriorates with the deviation of frequency because the amplitude and phase relation of the voltages of each nodes in the divider become worse.

Frequency characteristics of the divider depend on the admittance of the probe-pair $g_p + jb_p$ because (6)$\sim$(9) are used for the design. The dependance of -0.5dB-relative bandwidth r (the

Table I Maximum −0.5dB-relative bandwidth r and optimum g_p and b_p of the divider.

N(# of port)		1(4)	2(8)	3(12)	4(16)	5(20)
$b_p > 0$	g_p	1.2	0.7	0.5	0.3	0.3
	b_p	0.2	0.3	0.4	0.6	0.7
	r	0.36	0.20	0.32	0.24	0.22
$b_p < 0$	g_p	1.2	0.7	0.5	0.3	0.40
	b_p	−0.2	−0.1	−0.1	−0.2	−0.70
	r	0.32	0.18	0.32	0.18	0.16

Table II Parameters of the divider for experiments.

N	s	d_p	g_p	jb_p	g_c	jb_c	ϕ_c
1	3.2	8.0	1.25	$j0.68$	0.77	$j0.24$	1.49
2	3.2	7.0	0.66	$j0.54$	0.77	$j0.24$	1.39
3	3.2	6.5	0.47	$j0.47$	0.77	$j0.24$	1.32
4	4.0	5.6	0.42	$j0.47$	0.63	$j0.26$	1.30

Table III Measured characteristics of the dividers.

Number of ports ($4N$)	4	8	12	16
−0.5dB relative bandwidth	0.5	0.38	0.38	0.17
Insertion loss	Less than 0.1dB			

ratio of the band in which the insertion loss of the divider is within −0.5dB to the design frequency f_0) on the g_p and b_p was calculated. The result of 8–way divider is depicted in Fig. 4. Since connectors such as SMA's are to be used for the input/output port, the spacing between two neiboring probe-pairs ϕ_k has lower limitation in length. Table I shows the maximum −0.5dB-relative bandwidth and the optimum values of g_p and b_p with the limitation of $\phi_k \geq$ 1.2 rad ($2 \leq k \leq N$) at 9.0GHz. The maximum bandwidth on each steps do not have much differences between the design of $b_p > 0$ and $b_p < 0$, and decreases with the number of the steps N. Note that the wideband characteristics of 22% are obtained for $b_p > 0$, $N \leq 5$ divider, and wider bandwidth will be obtained by shortening the distances ϕ_c to around $\pi/2$.

Experiments for the power division

Experiments on divider/combiner's of $N = 1 \sim 4$ were carried out at X-band. The divider/combiner was designed at 9.0GHz, and the probe-pair whose g_p and b_p provides the maximum bandwidth was used. The parameters of divider/combiner's for experiments are listed in Table II. The center probe was designed by using (6),(7) and (11).

Fig. 3 shows the results of measurements on the 8–way divider, and measured −0.5dB-relative bandwidths for dividers of N=1∼4 are listed in Table III. Measured results indicate a good performance in good accordance with the theory : the insertion loss of $N \leq 4$ divider at 9.0GHz was less than 0.1dB, and −0.5dB-relative bandwidth, which is a little wider than the theoretical values, was 0.17 for N=4 and was wider for $N \leq 3$ dividers.

STABLE OPERATION OF THE POWER COMBINER

Combiner operation under phase deviation of input signals

The phase Ψ_k of input signal to the k-th probe-pair of the N-stage double-ladder combiner should satisfy the requirement (10). The phase deviation from (10) may be caused by unequality in unit-amplifiers, and the combining efficiency deteriorates with the deviation. The analysis of combiner operation under the input phase deviation are carried out using the equivalent circuit. In the analysis, Ψ_1=0 is assumed without loosing generalities. Analytical and experimental results for the 4–way combiner are depicted in Fig. 5. Both are in good accordance, and the deterioration of the combining efficiency is less than 0.1dB if the phases deviation is within ±17 deg. It was also revealed that the frequency characteristics depend little on the phase deviation. Further analysis of combiners with many more probe-pairs indicated that the phase deviation of input signals have little effects on the combining efficiency and the frequency characteristics.

Graceful degradation property

The graceful degradation property of a divider – unit-amplifier's – combiner system when some active devices breakdown is also discussed in terms of S-parameters. Let us denote S-parameters as $\{S_{ij}\}$ ($0 \leq i,j \leq N$, the input port is denoted as #0). In the case when #l port unit-amplifier breaks down as shown in Fig. 6, the gain of the amplifier system G is ex-

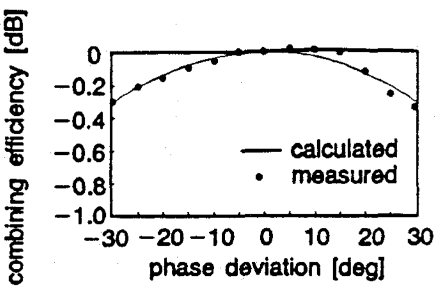

Fig. 5 Insertion loss.

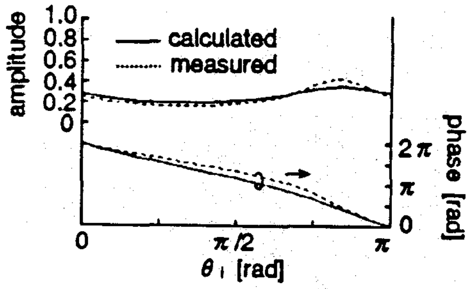

Fig. 7 Return loss.

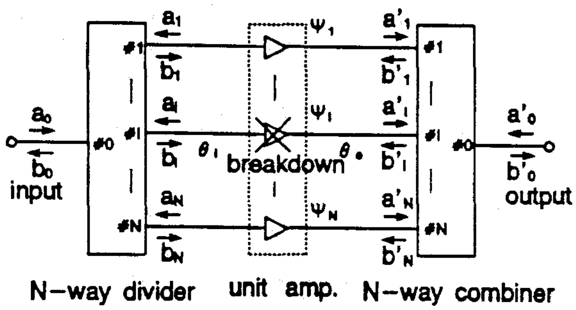

Fig. 6 Divider – unit-amplifier's – combiner system.

by

$$G = \sum_{k\neq l} S_{0k} a'_k + \frac{\sum_{k\neq l} S_{lk} a'_k}{1 - S_{ll}\Gamma_{ol}} S_{0l}\Gamma_{ol} \qquad (12)$$

where,

$$a'_k = \begin{cases} \left(S_{k0} + \dfrac{S_{kl}S_{l0}\Gamma_{il}}{1 - S_{ll}\Gamma_{il}}\right) A_k & (1 \le k \le N) \\ 0 & (k = 0). \end{cases} \qquad (13)$$

Γ_{il} is the reflection coefficient of the unit-amplifier looking from the output port of the divider, and Γ_{ol} is the reflection coefficient looking from the input port of the combiner, and A_k is power gain of the k-th unit-amplifier ($1 \le k \le N$), whose reverse gain is assumed zero. The return loss L is expressed by

$$L = S_{00} + \frac{S_{0l}S_{l0}\Gamma_{il}}{1 - S_{ll}\Gamma_{il}}. \qquad (14)$$

In the calculation, the gain of the unfailed unit-amplifier's is assumed to be unity and failed unit-amplifier is approximated by the short-circuited condition. Table IV shows the power gain (G) and return loss (L) of the amplifier system shown in Fig. 6 together with the optimum phase θ_i and θ_o of the reflection coefficients Γ_{il} and Γ_{ol}, respectively. The gain and the return

Table IV Gain and return loss of the amplifier system with a short-circuit failed unit-amplifier.

N	θ_i	θ_o	Gain	Return loss
4	0.65π	0.6π	$0.978 \sim 1.004$	$0.245 \sim 0.261$
8	0.1π	0.1π	$0.895 \sim 0.923$	$0.088 \sim 0.188$
12	0.85π	0.85π	$0.532 \sim 0.740$	$0.010 \sim 0.215$

loss strongly depends on θ_i and θ_o, but choice of proper phase angle will keep the deterioration to a minimum.

Experiments on 4-way divider with short-circuited failure in one port were carried out. Fig. 7 shows the return loss at the input port. Measured results indicate good accordance with the theory.

CONCLUSION

We proposed a microwave power divider/combiner with multiple-port double-ladder structure for use in high power solid state power amplifiers. Numerical analysis for $N = 1 \sim 4$ divider/combiner's were carried out so as to obtain the maximum bandwidth, and the wide-band characteristics of 22% in −0.5-dB relative bandwidth are obtained for 20–way divider. Experiments of N=1~4 divider/combiner were carried out at X-band, and measured results indecated a good performance in good accordance with the theory : the insertion loss of $N \le 4$ divider was less than 0.1dB, and −0.5dB-relative bandwidth was 17% for N=4, and was wider bandwidth for $N \le 3$ dividers. The analysis and measurements for the stable operation of the combiner was also carried out.

REFERENCE

[1] K. Fukui, S. Nogi, A. Sanada and S. Ohishi, "Ladder Type Microwave Power Divider/Combiner's," J.IEICE, J74-C-I, pp27-37, Jan. 1991.